REMARKS

Claims 1-34 are pending in the present application. In the Office Action, claims 1-34 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Nagaraj, et al (U.S. Patent No. 5,805,842). The Examiner's rejections are respectfully traversed.

With regard to independent claims 1 and 18, Applicants describe and claim a method and an apparatus, respectively, for executing a read request over a PCI bus. The method includes obtaining an access request from a queue, transferring, by a first DMA transfer, data from the main memory to a second memory on a first device, and transferring, by a second DMA transfer, the data from the second memory to a second device. The apparatus includes a queue for storing a read access request, a main memory for storing data to be transferred, and a buffer memory for buffer storage of the data, whereby data transfer to the buffer memory is accomplished by a first DMA transfer. The claimed apparatus also includes a device located on the PCI bus for receiving the data, whereby data transfer from the buffer memory to the device is accomplished by a second DMA transfer, and a finite state machine associated with the queue for selecting an access request.

With regard to independent claims 10 and 26, Applicants describe and claim a method and an apparatus, respectively, for executing a write request over a PCI bus. The method includes writing an access request to a queue, transferring, by a first DMA transfer, data from a second device to a second memory on a first device, and transferring, by a second DMA transfer, the data from the second memory to the main memory of the first device. The apparatus includes a queue for storing a write access request, a device located on a PCI bus for storing data to be transferred, and a main memory for receiving the data. The apparatus also includes a buffer memory for buffer storage of the data, whereby data transfer to the buffer memory is

accomplished by a first DMA transfer and data transfer from the buffer memory to the main memory is accomplished by a second DMA transfer, as well as a finite state machine associated with the queue for selecting an access request.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. That is, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. Third, there must be a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. A recent Federal Circuit case emphasizes that, in an obviousness situation, the prior art must disclose each and every element of the claimed invention, and that any motivation to combine or modify the prior art must be based upon a suggestion in the prior art. *In re Lee*, 61 U.S.P.Q.2d 143 (Fed. Cir. 2002). Conclusory

statements regarding common knowledge and common sense are insufficient to support a finding of obviousness. *Id.* at 1434-35.

Nagaraj is directed to enabling a Peripheral Component Interconnect (PCI) bus to support direct memory access (DMA) transfers. Nagaraj describes a Main Memory 210 coupled to a PCI bus 220, which is also coupled to a PCI I/O device 225 and a plurality of DMA devices 230a-n. The PCI I/O device 225 described by Nagaraj includes an internal storage element 340 and two DMA controllers 300, 310. See Nagaraj, Figures 2 and 3. In operation, the PCI I/O device 225 performs a DMA transfer operation, such as a read or a write, by splitting the DMA transfer operation into two PCI cycles, i.e. one memory cycle and one I/O cycle. See Nagaraj, col. 4, ll. 19-24. However, as admitted by the Examiner, Nagaraj does not describe first and second DMA transfers, as claimed by Applicants in independent claims 1, 10, 18, and 26.

The Examiner alleges that it would be obvious to modify the cited reference to arrive at the claimed invention. In support of this allegation, the Examiner notes that the cited reference teaches that the DMA operation may be split into two PCI cycles. However, Nagaraj states that the two PCI cycles are needed to perform the DMA transfer operation. See Nagaraj, col. 4, ll. 46-47. Thus, Applicants respectfully submit that Nagaraj describes performing a first DMA transfer using two PCI cycles and does not describe performing a second DMA transfer, as called for by the claims. For at least the aforementioned reasons, Applicants respectfully submit that the cited reference does not teach or suggest all the limitations of independent claims 1, 10, 18, and 26.

Moreover, Applicants respectfully submit that Nagaraj teaches away from the present invention. In particular, Nagaraj states that a single DMA transfer having two PCI cycles is needed. Thus, Nagaraj teaches away from using a first and a second DMA transfer. It is by now well established that teaching away by the prior art constitutes *prima facie* evidence that the

claimed invention is not obvious. *See, inter alia, In re Fine,* 5 U.S.P.Q.2d (BNA) 1596, 1599 (Fed. Cir. 1988); *In re Nielson*, 2 U.S.P.Q.2d (BNA) 1525, 1528 (Fed. Cir. 1987); *In re Hedges*, 228 U.S.P.Q. (BNA) 685, 687 (Fed. Cir. 1986).

For at least the aforementioned reasons, Applicants respectfully submit that independent claims 1, 10, 18, 26, and all claims depending therefore are not obvious over Nagaraj and request that the Examiner's rejections under 35 USC 103(a) be withdrawn.

Arguments with respect to other dependent claims have been noted. However, in view of the aforementioned arguments, these arguments are moot and therefore not specifically addressed. To the extent that characterizations of the prior art references or Applicants' claimed subject matter are not specifically addressed, it is to be understood that Applicants do not acquiesce to such characterization.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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